What is claimed is:

1. A coded binary sequence, comprising:

a first group of consecutive bits, the first group having first and second equally sized portions and representing a first logic level, the bits in the first portion each having a second logic level and the bits in the second portion each having a third logic level; and

a second group of consecutive bits, the second group having first and second equally sized portions and representing a fourth logic level, the bits in the first portion each having a fifth logic level and the bits in the second portion each having a sixth logic level.

2. The binary sequence of claim 1 wherein:

the first and second equally sized portions of the first group respectively comprise first and second halves of the first group; and

the first and second equally sized portions of the second group respectively comprise first and second halves of the second group.

3. The binary sequence of claim 1 wherein:

the first, second, third, and fifth logic levels equal logic 0; and

the fourth and sixth logic levels equal logic 1.

4. A coded binary sequence, comprising:

a first group of consecutive bits each having a first logic level, the first group representing a second logic level; and

a second group of consecutive bits, the second group having first and second portions and representing a third logic level, the bits in the first portion each having a fourth logic level and the bits in the second portion each having a fifth logic level.

5. The binary sequence of claim 4 wherein:
the first, second, and fourth logic levels equal logic 0;
and the third and fifth logic levels equal logic 1.

6. The binary sequence of claim 4 wherein the first and second groups each respectively comprise four consecutive bits.

7. The binary sequence of claim 4 wherein the first and second portions of the second group respectively comprises first and second halves of the second group.

8. A coded binary sequence, comprising:
a first group of four consecutive bits each having a first logic level, the first group representing a second logic level; and
a second group of four consecutive bits respectively having a third logic level, the third logic level, a fourth logic level, and the fourth logic level, the second group representing a fifth logic level.

9. The code word of claim 8 wherein:
the first, second, and third logic values equal a logic 0; and
the fourth and fifth logic values equal a logic 1.

10. A storage disk, comprising:
disk sectors operable to store application data; and
servo wedges that store servo data that includes,
a first group of consecutive bits, the first group having first and second equally sized portions and representing a first logic level, the bits in the first portion each having a second logic level and the bits in the second portion each having a third logic level; and
a second group of consecutive bits, the second group having first and second equally sized portions and representing a fourth logic level,

the bits in the first portion each having a fifth logic level and the bits in the second portion each having a sixth logic level.

11. A Viterbi detector operable to:

receive a signal that represents a binary sequence having a first group of consecutive bits each having a first logic level and a second group of consecutive bits, the second group having first and second portions, the bits in the first portion having the first logic level and the bits in the second portion having a second logic level, the first group representing the first logic level and the second group representing the second logic level; and

recover the binary sequence from the signal.

12. The Viterbi detector of claim 11 wherein the binary sequence comprises a coded binary sequence.

13. The Viterbi detector of claim 11 wherein:

the first logic level comprises a logic 0; and

the second logic level comprises a logic 1.

14. A servo circuit, comprising:

a sample circuit operable to generate samples of a signal that represents a coded binary sequence having a first group of consecutive bits each having a first logic level and a second group of consecutive bits, the second group having first and second portions, the bits in the first portion having the first logic level and the bits in the second portion having a second logic level, the first group representing the first logic level and the second group representing the second logic level; and

a Viterbi detector coupled to the sample circuit and operable to recover the coded binary sequence from the samples of the signal.

15. The servo circuit of claim 14, further comprising a decoder coupled to the Viterbi detector and operable to decode the recovered binary sequence.

16. A disk-drive system, comprising:

a data-storage disk having a surface, data sectors at respective locations of the surface, and servo wedges that store servo data that includes a first group of consecutive bits each having a first logic level and a second group having first and second portions of consecutive bits, the bits in the first portion having the first logic level and the bits in the third portion having a second logic level, the first group representing the first logic level and the second group representing the second logic level;

a motor coupled to and operable to rotate the disk;

a read head operable to generate a servo signal that represents the servo data and having a position with respect to the surface of the data-storage disk;

a read-head positioning circuit operable to move the read head over the surface of the disk; and

a servo circuit coupled to the read head and operable to recover the servo data from the servo signal.

17. The disk-drive system of claim 16 wherein the servo circuit comprises: a sample circuit operable to generate samples of the servo signal; and

a Viterbi detector coupled to the sample circuit and operable to recover the servo data from the samples of the servo signal.

18. The disk-drive system of claim 16 wherein the servo circuit comprises a decoder operable to decode the recovered servo data.

19. The disk-drive system of claim 16 wherein the read head comprises a read-write head.

20. A method, comprising:

coding a first logic level as a first group of consecutive bits, the first group having first and second equally sized portions, the bits in the first portion each having a second logic level and the bits in the second portion each having a third logic level; and

coding a fourth logic level as a second group of consecutive bits, the second group having first and second equally sized portions, the bits in the first portion each having a fifth logic level and the bits in the second portion each having a sixth logic level.

21. The method of claim 20 wherein:

the first, second, third, and fifth logic values equal a logic 0; and

the fourth and sixth logic values equal a logic 1.

22. The method of claim 20 wherein the coding comprises:

coding the first logic level as a first group of four consecutive bits; and

coding the fourth logic level as a second group of four consecutive bits.

23. The method of claim 20 wherein the first and second portions of the first group and the first and second portions of the second group respectively comprise first and second halves of the first and second groups.

24. A method, comprising:

coding a first bit of servo data as a first group of four consecutive bits each having a first logic level; and

coding a second bit of servo data as a second group of four consecutive bits respectively having the first logic level, the first logic level, a second logic level, and the second logic level.

25. The method of claim 24 wherein:
the first bit equals a logic 0; and
the second bit equals a logic 1.

26. The method of claim 24 wherein:
the first logic level equals a logic 0; and
the second logic level equals a logic 1.

27. A method, comprising:
writing a first code symbol into a servo wedge of a data-storage disk, the first code symbol having a length and representing a first logic level; and
writing a second code symbol into the servo wedge, the second code symbol having the length or approximately the length, a first portion, and a second portion, and representing a second logic level, the first portion having a different value than the second portion.

28. The method of claim 27 wherein:
the first and second code symbols each comprise a number of code bits; and
the lengths of the first and second code symbols are each less than the product of the number and a length of a servo-bit region.

29. The method of claim 27 wherein:
the first code symbol represents a logic 0; and
the second code symbol represents a logic 1.

30. The method of claim 27 wherein the first and second portions of the second code symbol are or are approximately half as long as the second code word.